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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,751	11/30/2006	Takayuki Matsui	S004-5836 (PCT)	1480

7590 04/14/2009

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EXAMINER	
DARE, RYAN A	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,751	MATSUI ET AL.	
	Examiner	Art Unit	
	RYAN DARE	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,8,9,12,13,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8,9,12,13,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-6, 8-9, 12-13 and 16-17 are pending in the application, and have been examined in the present Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 5-6, 8-9, 12-13 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu, US Patent 5,768,617.

4. With respect to claim 1, Liu teaches a memory interface device to control a memory access with respect to: a memory write unit to comply with a memory write procedure in which every time data is written into a memory every predetermined amount unit, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed; and a memory readout unit which reads the data from the memory, the memory interface device comprising:

write detection means for detecting the write of the predetermined amount unit of the data from the memory write unit into the memory, in col. 11, lines 14-16;

signal generation means for generating a signal to notify the memory write unit that the readout of the data from the memory has been completed, in a case where the write of the predetermined amount unit of the data is detected, in col. 12, lines 7-22;

data storage amount measurement means for measuring an amount of the data stored in the memory, in col. 11, lines 16-23; and

memory readout control means for generating an interrupt signal with respect to the memory readout unit, in a case where the stored data amount in the memory reaches a predetermined readout start storage amount, in col. 11, lines 16-32.

5. With respect to claim 2, Liu teaches a memory interface device to control a memory access with respect to: a memory write unit to comply with a memory write procedure in which every time data is written into a memory every predetermined amount unit, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed; and a memory readout unit which reads the data from the memory, the memory interface device comprising:

write detection means for detecting the write of the predetermined amount unit of the data from the memory write unit into the memory, in col. 11, lines 14-16;

signal generation means for generating a signal to notify the memory write unit that the readout of the data from the memory has been completed, in a case where the write of the predetermined amount unit of the data is detected, in col. 12, lines 7-22;

data storage amount measurement means for measuring an amount of the data stored in the memory, in col. 11, lines 16-23;

data processing means for reading the data from the memory to subject the data to predetermined processing, in col. 12, lines 7-22; and

memory readout control means for generating an interrupt signal with respect to the memory readout unit, in a case where the stored data amount in the memory reaches a predetermined readout start storage amount, in col. 11, lines 16-32.

6. Claim 5 is rejected using similar reasoning as claim 1.

7. With respect to claim 6, Lie teaches the memory interface method according to claim 5, further comprising:

a step of temporarily stopping the readout completion notice, in a case where the stored data amount in the memory reaches the predetermined readout start storage amount, in col. 11, lines 16-23.

8. With respect to claim 8, Liu teaches a memory interface device to control a memory access with respect to: a first memory write and readout unit to comply with a memory write procedure in which every time data is written into a memory every predetermined amount unit, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed; and a second memory write and readout unit which writes and reads the data with respect to the memory, the memory interface device comprising:

write detection means for detecting the write of the predetermined amount unit of the data from the first memory write and readout unit into the memory, in col. 11, lines 14-16;

first completion signal generation means for generating a signal to notify the first memory write and readout unit that the readout of the data from the memory has been completed, in a case where the write of the predetermined amount unit of the data is detected, in col. 12, lines 7-22;

first data storage amount measurement means for measuring an amount of the data stored in the memory, in col. 11, lines 16-23;

first memory readout control means for generating an interrupt signal with respect to the second memory write and readout unit, in a case where the stored data amount in the memory reaches a predetermined readout start storage amount;
write amount detection means for detecting the write of the predetermined amount of the data from the second memory write and readout unit into the memory, in col. 11, lines 16-32;

second completion signal generation means for generating a signal to notify the first memory write and readout unit that the write of the data into the memory has been completed, in a case where the write of the predetermined amount of the data is detected, in col. 11, lines 16-32;

second data storage amount measurement means for measurement the stored data amount in the memory, in col. 11, lines 16-32; and

second memory readout control means for generating an interrupt signal with respect to the second memory write and readout unit, in a case where the stored data amount in the memory reaches a predetermined readout completion storage amount, in col. 11, lines 16-32.

9. Claim 9 is rejected using similar reasoning as claim 6.

10. Claims 12-13 are rejected using similar reasoning as claims 8 and 9.

11. Claims 16-17 are rejected using similar reasoning as claims 1 and 8.

Conclusion

12. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar buffer write systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN DARE whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Dare/
April 10, 2009

/Pierre-Michel Bataille/
Primary Examiner, Art Unit 2186